REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. The specification has been amended to correct for minor informalities. The claims have been amended to correct for minor informalities, improve clarity, and improve antecedence. New dependent claims 24-49 have been added to more fully protect Applicant's invention. No new matter has been added.

OFFICE ACTION

In the Office Action mailed April 1, 2002 (hereinafter, the "OFFICE ACTION"), independent claims 1, 10 and 23, along with certain claims which depend therefrom were rejected as being obvious over U.S. Patent 4,977,498 to Rastegar et al., (hereinafter, "Rastegar") in view of Applicant's own disclosure (i.e., certain comments contained in the specification, hereinafter referred to as "Applicant's disclosure", see OFFICE ACTION, starting on Page 3).

In addition, independent claim 19 and claims which depend therefrom, as well as dependent claim 13 (which depends from independent claim 10) were rejected as being obvious over Rastegar in view of Applicant's disclosure and further in view of the presentation given by Poulton J. i.e., titled *Signaling in High Performance Memory Systems*, which was given at the IEEE Solid State Circuits Conferences in February of 1999 (hereinafter, "Poulton"). Applicants submit that none of the pending claims are obvious in

view of the cited combinations of Rastegar, Applicant's disclosure and Poulton.

It should be noted that, although not separately addressed herein, dependent claims 2-9, 11-18, 20-22, and 24 incorporate limitations that present patentable subject matter in their own right. In short, these limitations are also not obvious in view of the matter cited in the aforementioned rejections. However, in an attempt to present a more concise response to the OFFICE ACTION, only certain limitations or elements of independent claims 1, 10, 19 and 23 are discussed below. No inference or conclusion of any kind should be drawn from the absence of comments pertaining to other limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Finally, it is not clear what is meant by what appears to be the Examiner's characterization of Applicant's invention(s) (e.g., OFFICE ACTION, page 4, paragraph 3:

> Indeed, the Applicants' invention does not appear to be placement of buffers and plural memory devices on a memory module (since such is shown in their prior art figures and discussed in their specification as APA) but rather the use of PTP links to connect memory modules to a memory controller, an arrangement clearly taught by Rastegar.

Applicants note that other characterizations appear in the OFFICE ACTION (e.g., pages 3-8 of the OFFICE ACTION) and believe these characterizations may be misconstrued. No inference or conclusion should be drawn that Applicants agree, in any way, with the Examiner's characterization(s). Indeed, no inference or

conclusion of any kind should be drawn from the absence of Applicants' comment(s) pertaining to any of the Examiner's characterization(s).

Claims 1, 10, and 23 Are Not Obvious

Applicants submit that claims 1, 10, and 23 (in their amended or pre-amended form) are not obvious.

Applicants acknowledge the Examiners remark on page 4 of the OFFICE ACTION, i.e.,

> Rastegar does not teach that his memory modules include the claimed buffer and plural memory devices, but would have been obvious to the skilled artisan at the time of the invention to include a buffer and plural memory devices on each of Rastegar's memory modules since such devices were well known at the time of the invention as evidenced by the APA and since using the buffers in the memory modules provides a standard interface for the controller to communicate with, simplifying the controller's duties and providing enhanced control of the memory devices on the module as well-known in the art at the time.

Applicants respectfully disagree and submit that claim 1 is not rendered obvious by the combination of Rastegar and Applicant's disclosure.

It should be noted that Rastegar, to the extent understood, is unclear as to how modules 13 connect to the remainder of the memory system shown in Fig. 1. of Rastegar. In this regard, Rastegar states (emphasis added), "The memory system is also coupled, by a point to point bus arrangement, to multiple central processing

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units (hereinafter, CPU's)... The memory controller is coupled, by a point to point bus arrangement, to I/O devices or other memory systems." (col. 1, lines 42-51), and "bus 16" (col. 4, lines 7-8).

Notwithstanding the foregoing, applicants submit that it is non-obvious, (and counter intuitive) to include, for example, a buffer device i.e., incorporated between memory devices[1] on module 13 and the memory control box 13 ("MCB 13", Fig 1. of Rastegar). Rastegar teaches away from the concept of the buffer device, as is recited in the pending claims. In the memory system shown in Rastegar, employing point-to-point links[2] (to couple memory devices disposed on module 13 to MCB 13) would obviate motivation one skilled in the art would have to interpose buffer devices between module 13 and MCB 13, (i.e., such as reducing the capacitive loading which limits memory system bandwidth in a bus based memory system). For example, see page 5, lines 13-15 of the specification:

> The load capacitances connected to multiple points along the length of the signal line may degrade signaling performance. As more load capacitances are introduced

[1] Rastegar, to the extent understood, discloses no memory devices at all with the exception that such memory devices may be inherent on module 13, (Fig. 1 of Rastegar, see also col. 3, line 63, to col. 4, line 8). In addition, very little to no substantive detail of modules 13 are provided in Rastegar.

[2] Because, in the OFFICE ACTION, the examiner characterizes Rastegar as disclosing "point to point links", for brevity, Applicants herein make a hypothetical presumption that Rastegar discloses "point to point links" despite the fact that Rastegar also characterizes the connection between MCB 11 and modules 13 as "bus 16" - see col. 4, lines 7-8 of Rastegar i.e., "A bus 16 couples each of the memory modules 13 to the MCB 11". No inference or conclusion should be drawn that applicants agree that Rastegar discloses "point to point links".

along the signal line of the bus, signal settling time correspondingly decreases reducing the bandwidth of the memory system.

Thus for at least these reasons, claims 1, 10 and 23 (or the claims which depend therefrom) are not rendered obvious by the cited combination of Rastegar and Applicant's disclosure.

Claim 19 is Not Rendered Obvious by the Cited Matter

Applicants submit that claim 19 (in its amended or pre-amended form) is not obvious. Claim 19 was rejected as being obvious in view of the cited combinations of Rastegar, Applicant's disclosure and Poulton. Applicants respectfully disagree.

For reasons similar to the above with respect to claims 1, 10, and 23, applicants submit that claim 19 is not obvious in view of Rastegar, and Applicant's disclosure. With regard to the Examiner's reference to slide 57 of Poulton (page 7 of the OFFICE ACTION), there is no disclosure or teaching of incorporating buffer devices or repeater devices in a memory system as is recited in the pending claims. Rather, the few comments appearing on slide 57 teach away from this approach and suggest linking certain integrated circuit memory devices together (i.e., "DRAM"s captioned on slide 57 of Poulton) in various configurations, such as exclusively through the use of bi-directional serial links (i.e., here each DRAM includes 2 sets of differential input terminals and 2 sets of differential output terminals).

Thus, at least for the aforementioned reasons, claim 19 (or the claims which depend therefrom) is not obvious in view of the

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cited combinations of Rastegar, Applicant's disclosure and Poulton, since none of these, singly or in combination suggest, at the very least, the buffer device or the repeater device as they are portrayed in claim 19.

Information Disclosure Statement

Applicants have submitted concurrently herewith (via U.S. first class mail), an Information Disclosure Statement ("IDS"), and citation Form PTO/SB/08A along with a copies of the three (3) documents referenced therein. It is respectfully requested that the Examiner make his consideration of the IDS formally of record with the next Action. A copy of the IDS is attached hereto.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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ABSTRACT OF THE DISCLOSURE

A memory system architecture/interconnect topology that includes at least one point-to-point link between a master, and at least one memory subsystem. The memory subsystem includes a buffer device coupled to a plurality of memory devices. The memory system may be upgraded through dedicated point-to-point links and corresponding memory subsystems. The master communicates to the plurality of memory devices in each memory subsystem through the respective buffer device via each point-to-point link.

Exhibit A -- Version with Markings to Show Changes Made

1. (Amended) A memory system comprising:

a memory controller having an interface that includes a plurality of memory subsystem ports [including a first memory subsystem port];

a first memory subsystem including:

a buffer device having a first port and a second port, and

a plurality of memory devices coupled to the buffer device via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the memory controller via the buffer device;

and

a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link [connecting] to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports [to transfer data between the plurality of memory devices and the memory controller].

2. (Amended) The memory system of claim 1 further including:

a plurality of connectors, wherein each connector of the plurality of connectors is connected to a [connection to a] respective point-to-point link of the plurality of point-to-point links; and

a plurality of memory subsystems, and wherein each memory subsystem of the plurality of memory subsystems includes[including]:

a buffer device having a first port and a second port, wherein the first port is coupled to a respective connector of the plurality of connectors[,]; and

a plurality of memory devices coupled to the buffer device via the second port.

3. (Amended) The memory system of claim 2 further including a plurality of substrates wherein each memory subsystem of the plurality of memory subsystems is disposed on a respective substrate of the plurality of substrates.

4. (Amended) The memory system of claim 1 wherein [each of] the plurality of point-to-point links, first memory subsystem, and memory controller are disposed on [include] a common substrate.

5. (Amended) The memory system of claim 1 wherein the first memory subsystem further includes a plurality of channels and a plurality of memory device select lines connected between the plurality of memory devices and the second port.

6. The memory system of claim 5 wherein each channel includes a plurality of terminated signal lines.

7. (Amended) The memory system of claim 1 wherein the buffer device of the first memory subsystem further includes [at least one selected from the group consisting of a cache, a clock generator, and] a clock alignment circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

8. (Amended) The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of memory devices of the first memory subsystem and the memory controller [device].

9. (Amended) The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of buffer devices and the memory controller [device].

10. (Amended) A memory system comprising:
a controller device;
a first buffer device having a first interface and a second interface;
a second buffer device having a first interface and a second interface;
a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first buffer device;
a first [channel] plurality of memory devices connected to the second interface of the first buffer device;
[a first plurality of memory devices electrically coupled to the first channel];
a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second buffer; and
a second [channel] plurality of memory devices connected to the second interface of the second buffer device[; and
a second plurality of memory devices electrically coupled to the second channel].

11. (Amended) The memory system of claim 10, wherein the first buffer device [, first channel] and first plurality of memory devices are disposed on a first substrate, and the second buffer device [, second channel,] and second plurality of memory devices are disposed on a second substrate.

12. (Amended) The memory system of claim 11, further including:
a first plurality of signal lines to connect the first plurality of memory devices to the second interface of the first buffer device;
a second plurality of signal lines to connect the second plurality of memory devices to the second interface of the second buffer device;

[a plurality of termination elements disposed on each of the first and second substrate, wherein] a first plurality of termination elements connected to the first plurality of signal lines[are connected to the first channel,] and

a second plurality of termination elements connected to the second plurality of signal lines[are connected to the second channel].

13. (Amended) The memory system of claim 10, wherein the first buffer device further includes a third interface, the memory system further including:

a third buffer device having a first interface and a second interface;

a third point-to-point link having a first connection to the third interface and a second connection to the first interface of the third buffer device; and

a third plurality of memory devices [channel] connected to the second interface of the third buffer device[; and

a third plurality of memory devices electrically coupled to the third channel].

15. (Amended) The memory system of claim 10 further including:

a first channel to connect the first plurality of memory devices to the second interface of the first buffer device;

a second channel to connect the second plurality of memory devices to the second interface of the second buffer device;

a third channel connected to the second interface of the first buffer device;

a third plurality of memory devices electrically coupled to the third channel;

a fourth channel connected to the second interface of the second buffer device; and

a fourth plurality of memory devices electrically coupled to the fourth channel.

18. (Amended) The memory system of claim 10 wherein the first and second buffer devices each further include [at least one selected from the group consisting of a cache, a clock generator and] a clock alignment circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

20. (Amended) The memory system of claim 19, wherein each buffer device of the first and second plurality of buffer devices and corresponding plurality of memory devices are each disposed on [a] one of a plurality of respective module substrates.

21. (Amended) The memory system of claim 19 further including a third point-to-point link having an end connected to the controller device and a fourth point-to-point link having an end connected to the controller device.

22. (Amended) The memory system of claim 19 wherein each buffer device of the first and second plurality of buffer devices each further include [at least one selected from the group consisting of a cache, a clock generator, and] a clock alignment circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

23. (Amended) A memory system comprising:

a controller device having an interface;

a first connector, second connector, and third connector;

a first point-to point link having a first connection to the interface and a second connection to the first connector;

a second point-to-point link having a first connection to the interface and a second connection to the second connector;

a third point-to-point link having a first connection to the interface and a second connection to the third connector; and

a first memory subsystem including:

a buffer device [having a having a first interface]

connected to the first connector[, and a second interface]; and

a plurality of memory devices connected to the [second interface]buffer device, wherein at least one memory device of the plurality of memory devices transfer data to the controller device via the buffer device.

24. (Amended) The memory system of claim 23 wherein the second and third connectors support coupling to respective second and third memory subsystems.